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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,319	08/17/2001	Gerard Chauvel	TI-31357	5661

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	

ART UNIT	PAPER NUMBER
2188	15

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/932,319	Applicant(s) CHAUVEL, GERARD	
	Examiner Reginald G. Bragdon	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,14,15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,14 and 15* is/are rejected.

7)☒ Claim(s) *2-3 and 17-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason et al. (5,319,760) in view of Chang et al. (6,119,204).

As per claims 1 and 14, Mason et al. teaches a central processing system ("processor") which employs a translation buffer caching recently used page table entries ("TLB" or "storage circuitry"). See column 3, lines 55-56, and column 4, lines 41-44. With reference to figure 10, a virtual address is received on a set of inputs to the TB 48 and a physical address is output through selector 92 ("set of outputs"). The system of Mason et al. is a multitasking system, where several processes may reside in memory at the same time ("executing a plurality of program tasks within the processor" and "initiating a plurality of memory access requests in response to the plurality of program tasks"). See column 9, lines 11-13. As set forth in column 4, lines 41-44, recently used page table entries are cached in the translation buffer ("caching a plurality of translated memory addresses in the TLB responsive to the plurality of memory access requests").

The page table entries stored in the translation buffers 36 and 48 include an address space number field ("task identification value"), or ASN. See column 9, lines 35-36 and 47-51. The

address space number is loaded from the process control block (see column 9, lines 50-51) and therefore Mason et al. teaches that the ASN stored in the page table entries of the translation buffer "indicate which of the plurality of program tasks requested the respective translated memory address".

Mason et al. teaches that each page table entry 81 (figure 9) stores a bit called an "address space match" which allows the operating system to designate locations in the systems virtual address space which are shared among all processes ("incorporating a shared indicator with each translated memory address to indicate when a translated memory address is shared by more than one of the plurality of program tasks"). See column 11, line 65, to column 12, line 3.

Mason et al. further teaches flushing entries in the translation buffer when there is a context switch, where useful entries in the TB are not flushed (see column 9, lines 43-47) and the address space match bit ("shared indicator") is utilized determine if a particular entry should not be flushed (i.e. invalidated) on a context switch ("in a manner qualified by the shared indicator"). See column 2, lines 38-44, and column 11, lines 57-61. It is noted that a context switch, where the present invalidation occurs, does not change data in any other memory (i.e. the invalidation does not occur in response to a write operation).

Mason et al. does not teach an invalidate TLB entry command to initiate the invalidation of the TLB entries. Chang et al. teaches that it was known to invalidate TLB entries on a context switch using an explicit TLB invalidate instruction. See column 1, lines 60-61 and 63-67. It would have been obvious to one of ordinary skill in the art to have utilized a TLB invalidate command to invalidate the entries in the translation buffer of Mason et al., as taught by Chang et al., because Chang et al. suggests that a TLB invalidate command is an efficient mechanism for

initiating a TLB invalidation operation in software based coherency systems (see column 1, lines 64-66), such as the system of Mason et al., where the virtual memory system is managed by the operating system.

3. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Mason et al. and Chang et al. in view of Slater, "A Guide to RISC Microprocessors".

As per claim 15, the combination of Mason et al. and Chang et al. does not teach that the system has several levels of TLB and invalidating encompasses invalidating all of the levels of TLB. Slater teaches that it was known to include a "2nd" level of TLB, called the TLB slice, in addition to the traditional full TLB. See page 115. Slater also teaches that the TLB slice is updated along with the full TLB. See page 116, second full paragraph. It would have been obvious to one of ordinary skill in the art to have modified the combination of Mason et al. and Chang et al. to include a TLB slice as a second level of TLB, because Slater teaches that such an implementation would reduce the amount of transistors on the CPU chip.

Response to Arguments

4. Applicant's arguments filed 07 June 2004 have been fully considered but they are not persuasive.

Applicant argues that column 10, lines 7-11, of Mason et al. teaches that the address space number (ASN) and not the address space match bit (ASMB) conditions the operation of determining whether the tag (in the address translation) provides a match. The Examiner disagrees that column 10, lines 7-11, teaches away from the claim language of a "shared indicator" which "qualifies" the invalidating of TLB entries. As set forth in the rejection

previously, the ASMB (bit <4> of a page table entry) represents the "shared indicator" as taught at column 11, line 65, to column 12, line 3.

In the section of Mason et al. cited by Applicant (column 10, lines 7-11) if the ASMB is zero, the current ASN and the ASN of the PTE (field 94) must match for the address to be used and if the ASMB is one, then the ASN values are ignored. The ASMB qualifies whether the ASN are used in determining matching entries in the translation buffer.

It is noted that the term "qualifies" is a very broad term, and given its broadest reasonable interpretation, includes any and all links between the shared indicator and the invalidation operation. Applicant has not further defined the "qualifying" in claims 1 and 14.

Applicant argues that column 9, lines 51-68, of Mason et al. teaches that the conditional match based on the ASMB of column 10, lines 7-11, occurs during the normal operation of the translation buffer and does not teach determining whether to invalidate an entry. First the Examiner notes that the language of the claims sets forth using the shared indicator to "qualify" the invalidation, not "determine whether to invalidate an entry" as set forth by Applicant in the response at page 8.

Second, the ASMB is utilized in the invalidation process of the reference. Mason et al. sets forth that on a context switch, entries in the translation buffer are flushed (invalidated). See column 9, lines 43-47. Address space numbers are utilized to determine whether a particular entry in the translation buffer should be removed, since entries in the translation buffer not associated with the address space involved in the context switch do not need to be invalidated. See column 2, line 38-44 and column 11, lines 57-61. Based on the teachings of Mason et al. set forth above, shared entries in the translation buffer should not be removed from the translation

buffer since only process specific entries should be removed (column 11, lines 58-61). Based on this teaching, an entry with a ASMB indicating the entry is shared (see column 10, lines 7-11) should not be removed since the entry is shared and not "process specific". Therefore, Mason et al. suggests that the ASMB is used in determining whether an entry is shared and should therefore be invalidated or not.

Allowable Subject Matter

5. Claims 2-3 and 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
July 12, 2004